METHODS OF FABRICATING SEMICONDUCTOR DEVICES USING PRELIMINARY TRENCHES WITH EPITAXIAL GROWTH

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from Korean Patent Application No. 10-2010-0086072 filed on Sep. 2, 2010, in the Korean Intellectual Property Office, and all the benefits accruing therefrom under 35 U.S.C. 119, the contents of which in its entirety are herein incorporated by reference.

BACKGROUND

The present invention relates to the field of electronics, and more particularly, to method of fabricating semiconductor devices.

Recently, in order to increase the operating current of a semiconductor device, mechanical stress can be applied to the device to adjust the stress of a channel. That is to say, the operating current can be improved based on the principle that carrier mobility is affected when stress is applied to a channel.

When a compressive stress is applied to a channel region of a PMOS transistor, hole mobility is increased.

For example, a compressive stress may be applied to a channel region of a PMOS transistor by forming a trench in a source/drain region of a PMOS transistor and forming a SiGe layer in the trench. Here, the compressive stress applied to a channel region may be increased by forming the SiGe layer to be closer to the channel region.

SUMMARY

In some embodiments according to the inventive concept, methods of fabricating semiconductor devices using preliminary trenches with epitaxial growth can be provided. Related devices can also be provided. Pursuant to these embodiments, methods of fabricating a semiconductor device can be provided by forming a gate electrode on a substrate. A spacer can be formed on sidewalls of the gate electrode. A predetermined portion of the substrate exposed by the spacer and the gate electrode can be etched to form a first preliminary trench. A sacrificial layer can be formed on a bottom surface of the first preliminary trench. The sidewalls of the first preliminary trench exposed by the sacrificial layer can be laterally etched to form a second preliminary trench. The sacrificial layer can be removed and the second preliminary trench can be etched to form a trench. A SiGe epitaxial layer can be formed in the trench

In some embodiments according to the inventive concept, a method of fabricating a semiconductor device can be provided by etching sidewalls of a preliminary trench in a substrate that are between immediately adjacent gate electrode structures, to recess the sidewalls further beneath the gate electrode structures to provide recessed sidewalls. Then, the recessed sidewalls and a bottom of the preliminary trench can be etched using crystallographic anisotropic etching to form a hexagonally shaped trench in the substrate.

In some embodiments according to the inventive concept, the method can further include epitaxially growing a SiGe layer in the hexagonally shaped trench. In some embodiments according to the inventive concept, etching the recessed sidewalls can be provided by etching the recessed sidewalls to form outermost tips of the hexagonally shaped trench beneath the immediately adjacent gate electrode structures. In some embodiments according to the inventive concept, the outermost tips are aligned to sidewalls of the immediately adjacent gate electrode structures.

In some embodiments according to the inventive concept, the outermost tips are about 7 nm or less beneath a surface of the substrate.

In some embodiments according to the inventive concept, etching sidewalls of a preliminary trench is preceded by forming a sacrificial layer on a bottom surface preliminary trench. In some embodiments according to the inventive concept, forming a sacrificial layer on a bottom surface preliminary trench can be provided by forming the sacrificial layer on the bottom surface preliminary trench and exposing at least a portion of the sidewall of the preliminary trench.

In some embodiments according to the inventive concept, a semiconductor device can include immediately adjacent gate electrode structures on a substrate and a hexagonally shaped SiGe compressive strain layer in the substrate between the immediately adjacent gate electrode structures. The immediately adjacent gate electrode structures can include opposing sidewalls with outermost tips that extend beneath the immediately adjacent gate electrode structures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** to **7** and FIGS. **9** to **11** are cross-sectional views illustrating methods of fabricating semiconductor devices according to embodiments of the present invention,

FIG. **8** is an enlarged view of an 'A' portion of FIGS. **6** and **7**.

FIG. **12** illustrates a modified example of FIG. **11**.

FIGS. **13** to **15** are cross-sectional views illustrating intermediate stages in methods of fabricating semiconductor devices according to embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS ACCORDING TO THE INVENTIVE CONCEPT

Advantages and features of the present invention and methods of accomplishing the same may be understood more readily by reference to the following detailed description of preferred embodiments and the accompanying drawings. The present invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art, and the present invention will only be defined by the appended claims. In the drawings, the thickness of layers and regions are exaggerated for clarity.

It will be understood that when an element or layer is referred to as being "on" or "connected to" another element or layer, it can be directly on or connected to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on" or "directly connected to" another element or layer, there are no intervening elements or layers present. Like numbers refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

Spatially relative terms, such as "below," "beneath," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative